IDEC Chip Design Contest

Characterization of 28-nm MOSFET and Wire Devices for Cryogenic Computing

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I. Introduction

Cryogenic computing, which is to run the computer at extremely low temperature, is emerging as a breakthrough for next-generation high-performance computing. To understand the low-temperature behaviors of computing devices, researchers need to understand the low temperature behaviors of their basic block: MOSFET and wires.

In this project, we first manually design the MOSFET and wire samples and fabricate them with Samsung's 28nm technology. Next, with our semiconductor analyzer and probe station, we measure their characteristics at both the room temperature (i.e., 300K) and the cryogenic temperature (i.e.,77K). The measurement results can greatly contribute to developing more accurate models for cryogenic computing.

II. Design and Implementation

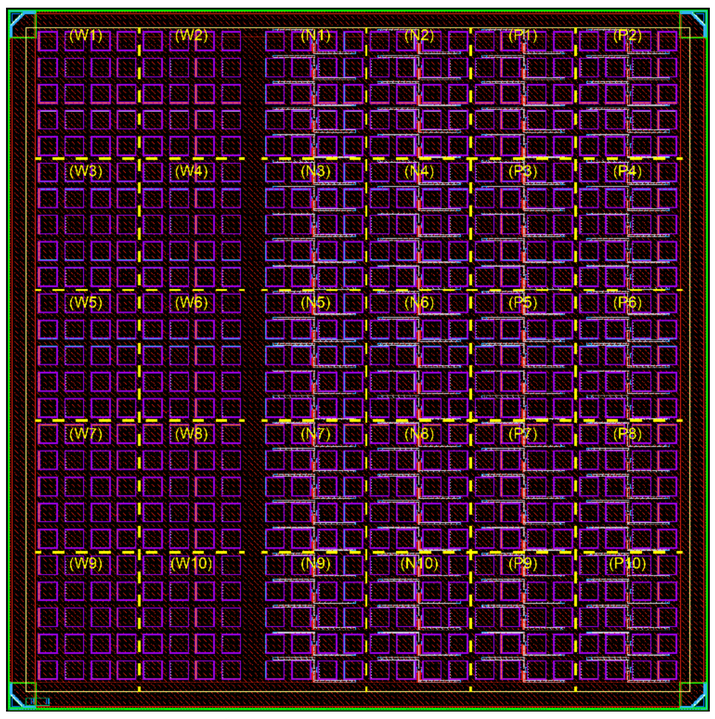


Figure 1. Layout of designed MOSFET and wire samples

Fig.1 shows the layout of the fabricated MOSFET and wire samples, which include 100 wire and 100 MOSFET samples with various wire length and gate width, respectively. For the wires, we fabricate ten types of wires whose wire lengths range from 200nm to 2000nm, with the 200nm interval (W1 to W10). For the MOSFETs, we fabricate ten types of NMOS/PMOS samples whose gate widths range from 80nm to 800nm with the 80nm interval (N1/P1 to N10/P10).

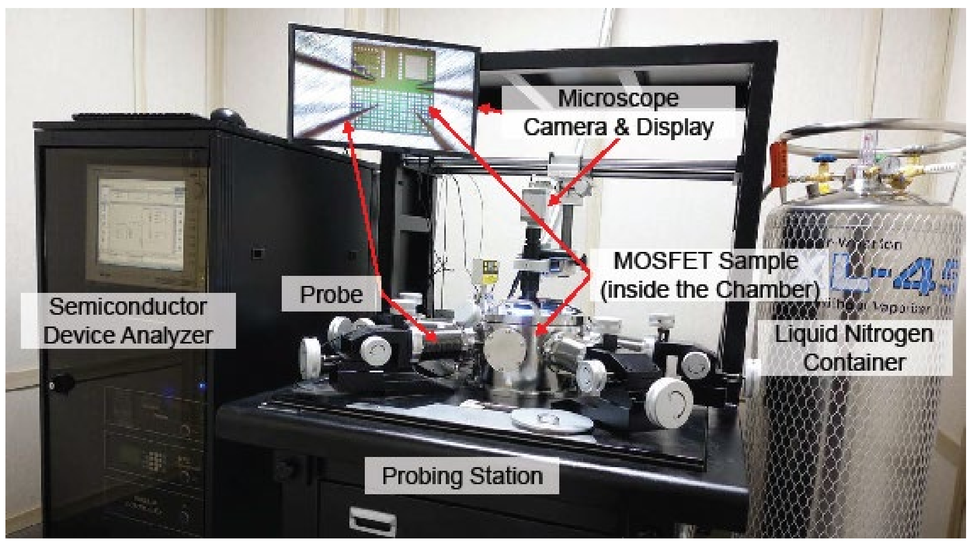
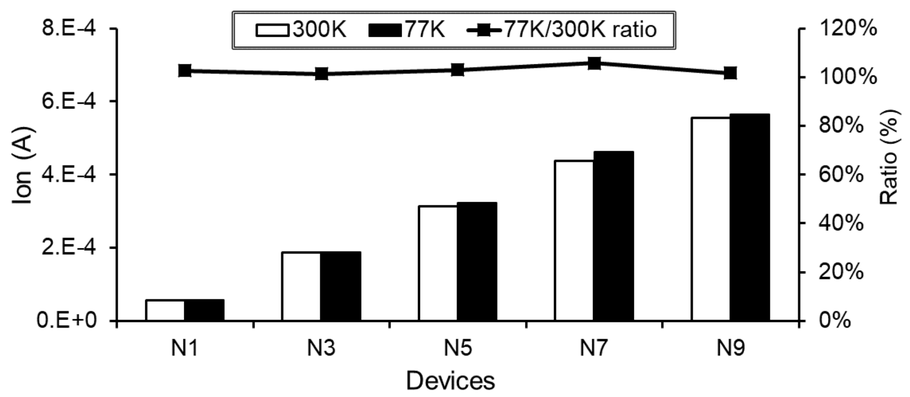


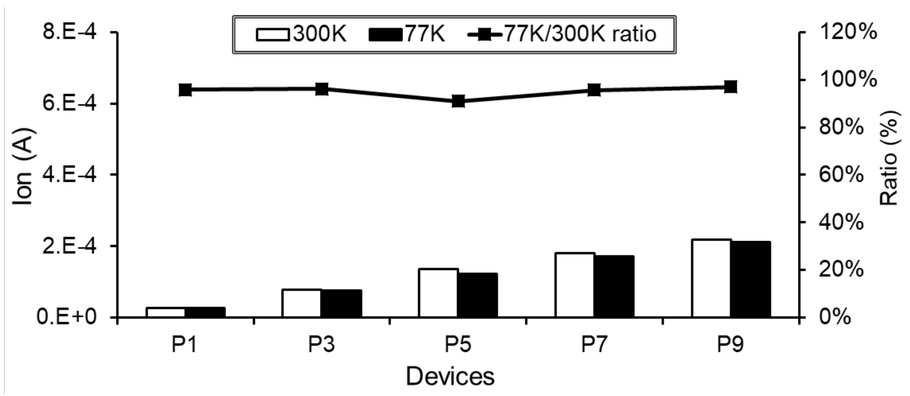
Figure 2. Experimental setup to measure MOSFET and wire samples at 77K

Fig.2 shows our measurement setup to measure the MOSFET and wire characteristics at 300K and 77K. We utilize a custom-built MOSFET probing station, which consists of a Keysight B1500A semiconductor device analyzer and a liquid nitrogen (LN)-based cooling unit.

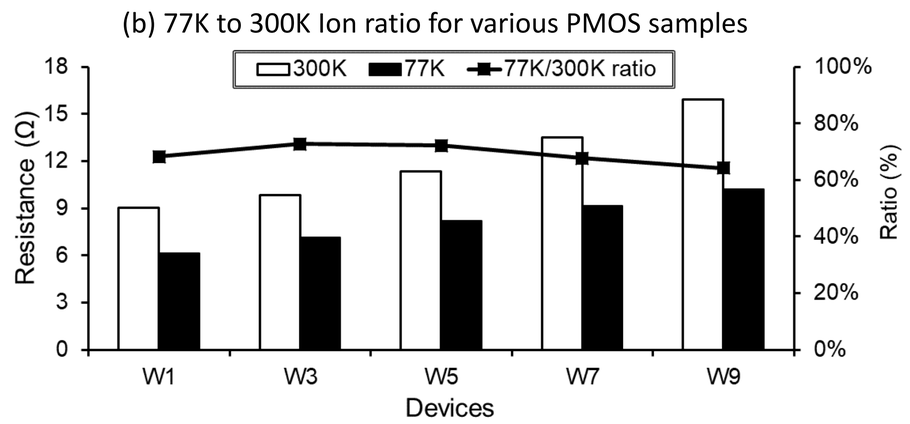
III. Measurement result



(a) 77K to 300K Ion ratio for various NMOS samples



(b) 77K to 300K Ion ratio for various PMOS samples



(c) 77K to 300K resistance ratio for various wire samples

Figure 3. measured 77K to 300K ratio for (a) NMOS, (b) PMOS and (c) wire samples

Fig.3 shows the measured 77K to 300K ratio for (a) NMOS, (b) PMOS, and (c) wire samples, respectively. We summarize our key observations as follows.

1. **NMOS at 77K.** As shown in Fig.3(a), we observed that the on-channel current (i.e., I_{on}) slightly increases with the temperature reduction. At 77K, the on-current of NMOS is % higher than 300K value on average. On the other hand, we observe that NMOS gate width does not meaningfully affect the temperature dependency of I_{on}, with 4.4% of maximum difference on 77K-to-300K ratio.
2. **PMOS at 77K.** As shown in Fig.3(b), we observed the different temperature dependence on I_{on} in PMOS devices. Specifically, the measured I_{on} at 77K is % lower than 300K value on average. However, for the dependency on gate width, we show the same trend on PMOS with NMOS devices. The maximum difference of I_{on} ratio for gate widths is at most 6%.
3. **Wire at 77K.** As shown in Fig.3(c), we observe that the wire resistance is greatly reduced at 77K, but the resistance reduction is much lower than that of bulk copper. The average wire resistance reduction is 31%, while the reduction in bulk copper is 85%. Therefore, we conclude that wire resistivity model should consider the physical wire width to accurately predict the resistivity at 77K.

IV. Conclusion

In this paper, we measure the MOSFET and wire characteristics at 77K, to help architects to build more accurate cryogenic MOSFET and wire models. We observe the slightly higher I_{on} for NMOS, slightly lower I_{on} for PMOS, and significantly reduced wire resistance at 77K, compared to 300K value.